IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

OPTi Inc.	)	
	)	
Plaintiff,	)	
v.	)	Civil Action No. 2:07CV021(TJW)
	)	
Apple, Inc.	)	
	)	
Defendant.	)	

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT

Pursuant to Patent Rule 4-3 of the Rules of Practice for Patent Cases and the Court's Amended Docket Control Order, the Parties hereby submit this Joint Claim Construction and Pre-hearing Statement.

(a) Agreed and Disputed Constructions and Evidence Relied Upon

The constructions agreed by the parties are set forth in Exhibit A to this Joint Statement. The first column of Exhibit A contains the language of the claims at issue. Limitations to be construed are indicated in **bold**.

The second and third columns include, respectively, OPTi's and Apple's proposed constructions. Where the parties have reached agreement on the limitations to be construed, those limitations are designated by a parenthetical as follows: (**Agreed-to Term)**. Otherwise, the parties' proposed constructions are set forth in their respective columns.

Plaintiff OPTi's intrinsic and extrinsic evidence in support of its proposed constructions and in opposition to Apple's is set forth in Exhibit B. Defendant Apple's intrinsic and extrinsic evidence in support of its proposed constructions and in opposition to OPTi's is set forth in

Exhibit C. The specifications of the two patents at issue are identical. For simplicity, all specification by both parties are to U.S. Patent 5,710,906.

For each of the patents-in-suit, the parties will jointly submit into evidence an agreed copy of the patents' files histories.

(b) Length of Time Needed for Claim Construction Hearing

The Parties agree that, in light of the complexity of the technology at issue, approximately 90 minutes (45 minutes per side) will be needed for the Claim Construction Hearing.

(c) Live Witnesses, Declarations, and Deposition Testimony

The parties do not currently plan to call live witnesses at the Claim Construction Hearing, unless the Court would find live testimony beneficial.

(d) Issues for Pre-Hearing Conference

The Parties do not currently foresee any disputes in need of resolution at a Pre-Hearing Conference. The Parties would be pleased to make themselves available at the Court's convenience should the Court believe that the Claim Construction Hearing would be facilitated by a Pre-Hearing Conference.

Dated: September 19, 2008

OPTi Inc.

By:

/s/ Michael L. Brody

Michael L. Brody
Taras A. Gracey
Ethan McComb
Sarah Frey
WINSTON & STRAWN LLP
35 West Wacker Dr.
Phone: (312) 558-5600
Fax: (312) 558-5700

mbrody@winston.com
tgracey@winston.com
emccomb@winston.com
sfrey@winston.com

Samuel F. Baxter
Gary Kitchen
MCKOOL SMITH, PC
104 E. Houston
Suite 300
Marshall, Texas 75670
Phone: (903) 923-9000
Fax: (903) 923-9099
sbaxter@mckoolsmith.com
gkitchen@mckoolsmith.com

Apple Inc.

/s/ Timothy S. Teter (with permission)

Timothy S. Teter
Matthew J. Brigham
Iain R. Cunningham
Cooley Godward Kronish LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663
teterts@cooley.com
mbrigham@cooley.com
icunningham@cooley.com

Eric M. Albritton
The Albritton Law Frim
P.O. Box 2649
Longview, TX 75606
Telephone: (903) 757-8449
Facsimile: (903) 758-7397

Danny L. Williams
Stephen Edwars
Williams, Morgan & Amerson
State Bar No. 21518050
10333 Richmond, Suite 1100
Houston, Texas 77042
Telephone: (713) 934-7000
Facsimile: (713) 934-7011
dwilliams@wmlaw.com

Exhibit A

Comparison of Proposed Claim Constructions

5,710,906		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**APPLE'S PROPOSED CONSTRUCTION**
Claim 9		
[9.1] A method for transferring data between a **bus master** and a plurality of memory locations at respective addresses in an address space of a **secondary memory**, for use with a host processing unit and a **first cache memory** which caches memory locations of said secondary memory for said host processing unit, **said first cache memory** having a line size of L bytes, comprising the steps of:	**"bus master" (Agreed-to Term)** an I/O-bus device that initiates a data transfer on an I/O bus	
	"first cache memory" (Agreed-to Term) the first level of cache memory, commonly referred to as L1 cache memory	
	"said first cache memory" (Agreed-to Term) *See* "first cache memory"	
	"secondary memory" (Agreed-to Term) memory located logically behind the first level cache memory, i.e., DRAM memory and, if present, L2 and L3 cache memory	
[9.2] **sequentially transferring at least three data units between said bus master and said secondary memory** beginning at a first starting memory location address in said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space; and	**"sequentially transferring at least three data units between said bus master and said secondary memory" (Agreed-to Term)** moving at least three data units between the bus master and the secondary memory in the sequence in which they are stored	
	"said bus master" (Agreed-to Term) *See* Limitation 9.1	
[9.3] **prior to completion of the transfer of the first data unit beyond said L-byte boundary**, **determining whether an N+1'th**	**"prior to the completion of the transfer of the first data unit beyond said L-byte boundary" (Agreed-to Term)** prior to completion of the transfer of the first data unit beyond said L-byte boundary	

<table>
<tr><th colspan="3">5,710,906</th></tr>
<tr><th>CLAIM LANGUAGE</th><th>OPTi'S PROPOSED CONSTRUCTION</th><th>APPLE'S PROPOSED CONSTRUCTION</th></tr>
<tr><td>L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary,</td><td>"determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory"

o determining whether the N+1th line of data in the first cache memory is different from the corresponding data in secondary memory</td><td>"determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory"

o determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory</td></tr>
<tr><td rowspan="3">[9.4] all of said transfers of data units in said step of sequentially transferring, occurring at a constant rate.</td><td colspan="2">"said transfers of data units in said step of sequentially transferring" (Agreed-to Term)
See Limitation 9.2</td></tr>
<tr><td colspan="2">" a constant rate" (Agreed-to Term)
a uniform rate</td></tr>
<tr><td>"all of said transfers of data units"

o each of the data unit transfers</td><td>"all of said transfers of data units"

o each and every one of the at least three transfers of data units</td></tr>
</table>

<table>
<tr><th colspan="3">6,405,291</th></tr>
<tr><th>CLAIM LANGUAGE</th><th>OPTi'S PROPOSED CONSTRUCTION</th><th>APPLE'S PROPOSED CONSTRUCTION</th></tr>
<tr><td>Claim 73</td><td></td><td></td></tr>
<tr><td rowspan="3">[73.1] A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a host processing unit and a cache memory which caches memory locations of said secondary memory for said host processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:</td><td colspan="2">"bus master" (Agreed-to Term)
See '906 Patent, Limitation 9.1</td></tr>
<tr><td colspan="2">"said bus master" (Agreed-to Term)
See '906 Patent, Limitation 9.1</td></tr>
<tr><td colspan="2">"secondary memory" (Agreed-to Term)
See '906 Patent, Limitation 9.1</td></tr>
<tr><td rowspan="2">[73.2] sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first and second L-byte boundaries of said secondary memory address space, each L-byte line of said transaction requiring at least 8 data unit transfers to said bus master; and</td><td colspan="2">"said bus master" (Agreed-to Term)
See '906 Patent, Limitation 9.1</td></tr>
<tr><td colspan="2">"sequentially transferring data units to said bus master from said secondary memory" (Agreed-to Term)
moving data units to the bus master from the secondary memory in the sequence in which they are stored</td></tr>
<tr><td>[73.3] during the transfer of the data units for each entire N'th L-byte line in said step of transferring, initiating one and only one snoop access of said cache memory, said</td><td colspan="2">"N+1'th L-byte line" (Agreed-to Term)
The next sequential line following line N</td></tr>
</table>

<table>
<tr><th colspan="3">6,405,291</th></tr>
<tr><th>CLAIM LANGUAGE</th><th>OPTi'S PROPOSED CONSTRUCTION</th><th>APPLE'S PROPOSED CONSTRUCTION</th></tr>
<tr><td rowspan="3">snoop accesses each specifying the respective N+1'th L-byte line and being initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line,</td><td colspan="2">"during the transfer of the data units for each entire N'th L-byte line" (Agreed-to Term)
While the data units for each entire N'th L-byte line are moving to the bus master from the secondary memory</td></tr>
<tr><td colspan="2">"the transfer of the data units" (Agreed-to Term)
See Limitation 73.2</td></tr>
<tr><td>"initiating one and only one snoop access of said cache memory"

o initiating one and only one next-line inquiry of said cache memory

"snoop access"

o next-line inquiry

o "inquiry" – an operation for determining whether a line of data in the first cache memory is different from the corresponding data in the secondary memory (Agreed-to Term)</td><td>"initiating one and only one snoop access of said cache memory"

o initiating one and only one snoop access of said cache memory

"snoop access"

o inquiry

o "inquiry" – an operation for determining whether a line of data in the first cache memory is different from the corresponding data in the secondary memory (Agreed-to Term)</td></tr>
<tr><td rowspan="2">[73.4] wherein said step of transferring comprises the step of transferring to said bus master three sequential data units including the last data unit before said first L-byte boundary and the first data unit beyond said first L-byte line, all at a constant rate,</td><td colspan="2">"said step of transferring" (Agreed-to Term)
See Limitation 73.2</td></tr>
<tr><td colspan="2">"constant rate" (Agreed-to Term)
See '906 Patent, Limitation 9.4</td></tr>
</table>

6,405,291		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**APPLE'S PROPOSED CONSTRUCTION**
[73.5] and wherein **said step of transferring** further comprises the step of transferring to said bus master three sequential data units including the last data unit before said second L-byte boundary and the first data unit beyond said second L-byte line, all at a **constant rate**.	**"said step of transferring" (Agreed-to Term)** *See* Limitation 73.2	
Claim 74		
[74.1] A method according to claim 73, wherein **said step of sequentially transferring data units** continues further beyond a third L-byte boundary of said **secondary memory**, and wherein **said step of transferring** further comprises the step of transferring three sequential data units including the last data unit before said third L-byte boundary and the first data unit beyond said third L-byte line, all at a **constant rate**.	**"said step of sequentially transferring data units" (Agreed-to Term)** *See* Limitation 73.2	
	"said step of transferring" (Agreed-to Term) *See* Limitation 73.2	
	"constant rate" (Agreed-to Term) *See* '906 Patent, Limitation 9.4	
Claim 88		
[88.1] **Controller apparatus for a computer** system which includes a **secondary memory** having an address space, a **bus master**, a host processing unit and a **cache memory** which caches memory locations of said secondary memory for said host processing unit, **said cache memory** having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to **said bus master** in parallel, said controller apparatus	**"bus master" (Agreed-to Term)** *See* '906 Patent, Limitation 9.1	
	"said bus master" (Agreed-to Term) *See* '906 Patent, Limitation 9.1	
	"cache memory" (Agreed-to Term) *See* Limitation 73.1	
	"said cache memory" (Agreed-to Term) *See* Limitation 73.1	

6,405,291		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**APPLE'S PROPOSED CONSTRUCTION**
comprising circuitry which in a mode of operation, in response to a PCI-bus burst read transaction initiated by said bus master,	**"secondary memory" (Agreed-to Term)** *See* '906 Patent, Limitation 9.1	
[88.2] **sequentially transfers data units to said bus master from said secondary memory** according to said PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first, second and third L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, a plurality of sequential data units bracketing at least said first, second and third L-byte boundaries being transferred to said bus master **at a constant rate**, said **constant rate** being dependent upon the frequency of a PCI-bus clock provided to said bus master; and	**"sequentially transfers data units to said bus master from said secondary memory" (Agreed-to Term)** moving data units to the bus master from the secondary memory in the sequence in which they are stored	
	"constant rate" (Agreed-to Term) *See* '906 Patent, Limitation 9.4	
	"at a constant rate" (Agreed-to Term) *See* '906 Patent, Limitation 9.4	
	(Agreed-to Construction) Not a means-plus-function element	
[88.3] **during the transfer of the data units for each entire N'th L-byte line according to said transaction**, **initiates one and only one snoop access** of said cache memory, said snoop access specifying the respective N+1'th L-byte line and being initiated early enough such that it can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line, said snoop	**"N+1'th L-byte line" (Agreed-to Term)** *See* Limitation 73.3	
	"during the transfer of the data units for each entire N'th L-byte line" (Agreed-to Term) *See* Limitation 73.3	
	(Agreed-to Construction) Not a means-plus-function element	

6,405,291		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**APPLE'S PROPOSED CONSTRUCTION**
accesses being sampled by said host processing unit in accordance with a host clock signal having a frequency that is at least twice said PCI-bus clock frequency.	**"initiates one and only one snoop access"** o *See* Limitation 73.3	**"initiates one and only one snoop access"** o *See* Limitation 73.3.

Exhibit B

OPTi's Intrinsic and Extrinsic Evidence

5,710,906		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**OPTi's EVIDENCE**
Claim 9		
[9.3] **"determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory"**	determining whether the N+1th line of data in the first cache memory is different from the corresponding data in secondary memory	3:24-4:46; 5:16-22; 6:7-23; 7:64-8:8; 8:36-9:10; 14:36-49; 15:1-16 PCI Local Bus Specification Rev. 2.0 (April 30, 1993) §§3.8, 3.8.1, 3.8.1.1, and 3.8.3. Shanley and Anderson, *PCI System Architecture* (Mindshare, Inc. 1995) GLOSSARY "Snooping" at 546. *AMD Markman Order*, Limitation 9.3 referring to Limitation 1.3 *NVIDIA Markman Order*, at 24-25.
[9.4] **"all of said transfers of data units"**	each of the data unit transfers	*AMD Markman Order*, Limitation 9.2, 9.4.

6,405,291		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**OPTi'S EVIDENCE**
Claim 73		
[73.1] **"secondary memory"**	*See* '906 Patent, Limitation 9.1	*See* '906 Patent, Limitation 9.1
[73.3] **"initiating one and only one snoop access of said cache memory"**	initiating one and only one next-line inquiry of said cache memory	4:20-46; 5:16-40; 6:7-41; 7:64-8:8; 8:36-9:10; 14:36-15:16; 20:64-24:35; Figs. 4, 8, and 9 '291 Prosecution History, Information Request for Further Examination, OPTIAPPLE 000355-387; Declaration of Subhir Ghosh, OPTIAPPLE 00334-354, Notice of Allowability at OPTIAPPLE 000329-330. AMD *Markman* Order, Limitation 1.3, 73.3; *nVidia Markman* Order, Limitation 4 at p. 24. Shanley and Anderson, *PCI System Architecture* (Mindshare, Inc. 1995) GLOSSARY "Snooping" at 546.
[73.3] **"snoop access"**	Next-line inquiry	4:20-5:22; 6:7-41. PCI Local Bus Specification Rev. 2.0 (April 30, 1993) §§3.8, 3.8.1, 3.8.1.1, and 3.8.3. *Pentium Processor User's Manual Vol. 1: Pentium Processor Data Book* (1993) § 3.7.7.1.3. Shanley and Anderson, *PCI System Architecture* (Mindshare, Inc. 1995) GLOSSARY

6,405,291		
CLAIM LANGUAGE	**OPTi'S PROPOSED CONSTRUCTION**	**OPTi'S EVIDENCE**
		"Snooping" at 546. AMD *Markman* Order, Limitation 73.3; nVidia *Markman* Order, Limitation 4 at p. 24.
Claim 88		
[88.3] **"initiates one and only one snoop access"**	*See* Limitation 73.3	*See* Limitation 73.3

Exhibit C

Apple's Intrinsic and Extrinsic Evidence

5,710,906		
CLAIM LANGUAGE	**APPLE'S PROPOSED CONSTRUCTION**	**APPLE'S EVIDENCE**
Claim 9		
[9.3] **"determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory"**	determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory	'906 Claim 10, 20. '906 Col. 4:28-32. '906 Col. 6:35-41. Shanley and Anderson, *PCI System Architecture* (Mindshare, Inc. 1995) GLOSSARY "Snooping" at 546.
[9.4] **"all of said transfers of data units"**	each and every one of the at least three transfers of data units	'906 Claim 9 ("sequentially transferring at least three data units between said bus master and said secondary memory")

6,405,291		
CLAIM LANGUAGE	**APPLE'S PROPOSED CONSTRUCTION**	**APPLE'S EVIDENCE**
Claim 73		
[73.3] **"initiating one and only one snoop access of said cache memory"**	initiating one and only one snoop access of said cache memory	Request for Further Consideration of IDS Documents D2-1 through D2-7 at 26-27 (Dec. 10, 2001) (distinguishing '291 Claims 73 and 88 (original numbering 74 and 89)). Declaration of Subir Ghosh in Support of Request for Further Consideration of IDS Documents D2-1 through D2-7, ¶52 (Dec. 10, 2001) ("52. Another feature incorporated into certain embodiments of our invention is that *one and only one* snoop access of the host cache is initiated during the transfer of the data units for each entire cache line of a transaction. This limitation is important because, among other things, a chipset that asserts multiple snoop accesses for each cache line transferred can tend to choke the processor and reduce the performance of the overall system."). '906 Fig. 4. *See also* '291 Claim 10, Claim 28, Claim 32, Claim 38, Claim 48. *See* below for evidence supporting definition of "snoop access."

6,405,291		
CLAIM LANGUAGE	**APPLE'S PROPOSED CONSTRUCTION**	**APPLE'S EVIDENCE**
[73.3] **"snoop access"**	inquiry	AMD Markman Order at 2-3 (inquiry: "an operation for determining whether a line of data in the first cache memory is different from the corresponding data in the secondary memory.") '906 Col. 4:28-32 ("Write-back cache controllers, therefore, typically support inquire cycles (also known as snoop cycles), in which a bus master asks the cache memory to indicate whether it has a more current copy of the data."). '906 Summary of the Invention, Col. 6:8-13 ("According to the invention, roughly described, when a PCI-bus controller receives a request from a PCI-bus master to transfer data with an address in secondary memory, the controller performs an initial inquire cycle and withholds TRDY# to the PCI-bus master until any write-back cycle completes.") '906 Col. 6:37-41 ("The invention is useful whenever an L1 cache is present which can use a write back protocol, and which supports inquire cycles, and whenever an I/O bus is present which has a linear-incrementing capability or mode which can continue beyond an L1 cache line boundary.") '906 Col. 7:64-8:2 ("Because at least one line of L1 cache 212 supports a write-back protocol,

6,405,291		
CLAIM LANGUAGE	**APPLE'S PROPOSED CONSTRUCTION**	**APPLE'S EVIDENCE**
		the host processing subsystem 110 also supports inquire cycles, initiated by the external system to determine whether a line of secondary memory is currently being cached in the L1 cache 212 and whether it has been modified in that cache.") *See also OPTi v. AMD* Proposed Claim Construction, PR 4-3 Chart at 2-3 (OPTi's constructions of "inquiry" and "next-line inquiry"). Shanley and Anderson, PCI System Architecture (Mindshare, Inc. 1995) GLOSSARY "Snooping" at 546 ("[t]he cache controller must snoop the transaction to determine if the current master is accessing information that is also resident within the cache.")
Claim 88		
[88.3] **"initiates one and only one snoop access"**	*See* Limitation 73.3	*See* Limitation 73.3